01-03-00

A

jc688 U.S. PTO 12/30/99

Please type a plus sign (+) inside this box [+]

PTO/SB/05 (12/97)
Approved for use through 09/30/00. OMB 0651-0032
Patent and Trademark Office: U.S. DEPARTMENT OF COMMERCE
Under the Paperwork Reduction Act of 1995, no persons are required to respond to a collection of information unless it displays a valid OMB control number.

jc525 U.S. PTO 09/475643 12/30/99

UTILITY PATENT APPLICATION TRANSMITTAL

(Only for new nonprovisional applications under 37 CFR 1.53(b)

Attorney Docket No. 042390.P7143 Total Pages 3

First Named Inventor or Application Identifier Michael J. Jassowski

Express Mail Label No. EL 431 887 326 US

ADDRESS TO:	**Assistant Commissioner for Patents** **Box Patent Application** **Washington, D. C. 20231**

APPLICATION ELEMENTS

See MPEP chapter 600 concerning utility patent application contents.

1. X Fee Transmittal Form
   (Submit an original, and a duplicate for fee processing)

2. X Specification (Total Pages 13)
   (preferred arrangement set forth below)
   - Descriptive Title of the Invention
   - Cross References to Related Applications
   - Statement Regarding Fed sponsored R & D
   - Reference to Microfiche Appendix
   - Background of the Invention
   - Brief Summary of the Invention
   - Brief Description of the Drawings (if filed)
   - Detailed Description
   - Claims
   - Abstract of the Disclosure

3. X Drawings(s) (35 USC 113) (Total Sheets 4)

4. X Oath or Declaration (Total Pages 5)
   a. ___ Newly Executed (Original or Copy)
   b. ___ Copy from a Prior Application (37 CFR 1.63(d))
   (for Continuation/Divisional with Box 17 completed) **(Note Box 5 below)**
   i. ___ DELETIONS OF INVENTOR(S) Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).

5. ____ Incorporation By Reference (useable if Box 4b is checked)
   The entire disclosure of the prior application, from which a copy of the oath or declaration is supplied under Box 4b, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

6. ____ Microfiche Computer Program (Appendix)

7. ____ Nucleotide and/or Amino Acid Sequence Submission

(if applicable, all necessary)

a. ____ Computer Readable Copy
b. ____ Paper Copy (identical to computer copy)
c. ____ Statement verifying identity of above copies

ACCOMPANYING APPLICATION PARTS

8. _____ Assignment Papers (cover sheet & documents(s))
9. _____ a. 37 CFR 3.73(b) Statement (where there is an assignee)

_X_ b. Power of Attorney

10. _____ English Translation Document (if applicable)
11. _____ a. Information Disclosure Statement (IDS)/PTO-1449

_____ b. Copies of IDS Citations

12. _____ Preliminary Amendment
13. _X_ Return Receipt Postcard (MPEP 503) (Should be specifically itemized)
14. _____ a. Small Entity Statement(s)

b. Statement filed in prior application, Status still proper and desired

15. _____ Certified Copy of Priority Document(s) (if foreign priority is claimed)

16. _X_ Other: Certificate of Express Mail with copy of postcard showing contents of Express Mail package.

17. **If a CONTINUING APPLICATION,** check appropriate box and supply the requisite information:

___ Continuation ____ Divisional ____ Continuation-in-part (CIP)

of prior application No: _____

18. **Correspondence Address**

_____ Customer Number or Bar Code Label _____
(Insert Customer No. or Attach Bar Code Label here)

or

_X_ Correspondence Address Below

NAME John P. Ward Reg No.: 40,216

BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP

ADDRESS 12400 Wilshire Boulevard

Seventh Floor

CITY Los Angeles STATE California ZIP CODE 90025-1026

Country U.S.A. TELEPHONE (408) 720-8598 FAX (408) 720-9397

PTO/SB/05 (12/97)
Approved for use through 09/30/00. OMB 0651-0032
Patent and Trademark Office; U.S. DEPARTMENT OF COMMERCE

Attorney Docket No. 42390.P7143

APPLICATION FOR UNITED STATES PATENT

FOR

OPTIMIZED DRIVER LAYOUT FOR INTEGRATED CIRCUITS WITH STAGGERED BOND PADS

Inventor: Michael A. Jassowski

Prepared by: Blakely, Sokoloff, Taylor & Zafman
12400 Wilshire Blvd. 7th Floor
Los Angeles, CA 90025-1026
(408) 720-8598

"Express Mail" mailing label number: EL 431 887 326 US
Date of Deposit: December 30, 1999
I hereby certify that I am causing this paper or fee to be deposited with the United States Postal Service "Express Mail Post Office to Addressee" service on the date indicated above and that this paper or fee has been addressed to the Assistant Commissioner for Patents, Washington, D. C. 20231

Lisa Kaiser
(Typed or printed name of person mailing paper or fee)

Lisa Kaiser
(Signature of person mailing paper or fee)

December 30, 1999
(Date signed)

OPTIMIZED DRIVER LAYOUT FOR INTEGRATED CIRCUITS WITH STAGGERED BOND PADS

Field Of The Invention

The present invention pertains to the field of computer systems. More particularly, this invention pertains to the field of integrated circuits with staggered bond pads.

Background of the Invention

Figure 1 shows a cross-sectional view of a portion of a typical ball grid array semiconductor device 100. Among the components of the typical ball grid array semiconductor device 100 is a die 110. The die 110 is coupled to a lead frame 120 via a bond wire 115. Although only a single bond wire is shown in figure 1, a typical semiconductor device may include dozens or hundreds of such bond wires. The lead frame 120 provides electrical pathways from the bond wires to the solder balls 140. Although this example shows only three solder balls, a typical ball grid array semiconductor device may include dozens or hundreds of such solder balls. A solder mask 150 provides electrical isolation between the various solder balls 140. The entire assembly is encapsulated in a plastic casing 130.

Figure 2 is a block diagram of a portion of a prior integrated circuit die with staggered bond pads. The staggered bond pads are represented by blocks 210 through 217. The bond pads are arrayed in close proximity to the edge of the die (indicated by line 260). Although only eight bond pads are depicted in figure 2, a typical prior integrated circuit with staggered bond pads may include hundreds of such bond pads. The bond pads 210 through 217 when assembled into a complete semiconductor device would be connected to a lead frame via bond wires, as seen in the example of figure 1.

The bond pads 210 through 217 are electrically coupled to a series of driver/ESD circuit cells 220 through 227. The term "ESD" refers to "electrostatic discharge". The driver/ESD cells 220 through 227 provide drive strength for output signals, receive input signals, and also provide ESD protection. The driver/ESD cells 220 through 227 are coupled to the bond pads 210 through 217 via metal connections. Two of the metal connections are labeled 240 and 247. Metal connection 240 connects bond pad 210 to driver/ESD cell 220, and metal connection 247 connects bond pad 217 to driver/ESD cell 227. The driver/ESD cells 220 through 227 are connected to a series of pre-driver cells 230 through 237. These cells serve to couple the driver/ESD cells with the circuitry located at the die core.

Because the bond pads 210 through 217 are arranged in a staggered array, with an inner ring including bond pads 211, 213, 215, and 217 and with an outer ring including bond pads 210, 212, 214, and 216, the metal connections to the outer ring bond pads must be routed between the inner ring bond pads.

It is often advantageous for a semiconductor device manufacturer to reduce the size of a die in an effort to produce more devices per wafer, thus reducing manufacturing costs per device. If the number of bond pads on the die is not to decrease, then the bond pads must be placed in closer proximity one to another when the size of the die is reduced. This, in turn, results in a more narrow metal connection between the driver/ESD cells and the bond pads in the outer ring. Also, the width of the driver/ESD cells is reduced.

Several problems can arise as the width of the metal connections between the driver/ESD cells and the bond pads in the outer ring is reduced. A more narrow metal

connection results in greater electrical resistance. The narrow connection may not be able to handle large currents that may occur as a result of an ESD event. The narrow metal connection may also experience electro-migration, which is a gradual erosion of the metal resulting in eventual circuit failure. One potential solution to the narrow metal connection problem may be to route additional metal on layers below the inner row of bond pads, but this potential solution raises a manufacturing problem of dielectric material that is typically deposited between metal layers cracking below the bond pads during installation of the bond wires.

In addition to the problems raised due to a reduction in width of the metal connections between the driver/ESD cells and the bond pads in the outer ring, a reduction in the width of the driver/ESD cells may make implementation of ESD protection structures within the driver/ESD cells more problematic.

Brief Description of the Drawings

The invention will be understood more fully from the detailed description given below and from the accompanying drawings of embodiments of the invention which, however, should not be taken to limit the invention to the specific embodiments described, but are for explanation and understanding only.

Figure 1 is a cross-sectional view of a typical ball grid array semiconductor device.

Figure 2 is a block diagram of a portion of a prior art semiconductor die.

Figure 3 is a block diagram of a portion of an embodiment of a semiconductor die configured in accordance with the invention.

Figure 4 is a flow diagram of an embodiment of a method for optimizing driver layout for integrated circuits with staggered bond pads.

Detailed Description

An embodiment of an integrated circuit die with staggered bond pads and optimized driver layout includes a staggered array of bond pads with an outer ring of bond pads and an inner ring of bond pads. Driver/ESD circuit cells for the outer ring of bond pads are located to the outside of the bond pads (between the outer ring of bond pads and the nearest die edge). The driver/ESD cells for the inner ring of bond pads are located to the inside of the bond pads.

Figure 3 is block diagram of an embodiment of a staggered bond pad integrated circuit die 300 with optimized driver layout. The die 300 includes pre-driver/receiver circuit cells 330 through 337. The pre-driver/receiver cells 330 through 337 provide communication between the die core and a series of driver/ESD circuit cells 320 through 327. The driver/ESD circuit cells 320 through 327 provide drive strength, receive incoming signals, and provide ESD protection. The driver/ESD circuit cells 320 through 327 are coupled to bond pads 310 through 317. The driver/ESD circuit cells and the bond pads are connected via a series of metal connections, two of which are labeled 340 and 347. Although only eight bond pads, eight driver/ESD cells, and eight pre-driver/receiver cells are shown in figure 3 in order to avoid obscuring the invention, embodiments of the invention are possible with many more bond pads, driver/ESD cells, and pre-driver/receiver cells. Further, the driver/ESD cells 320 through 327 are meant to represent a broad range of possible input/output cell circuits.

The driver/ESD cells 320, 322, 324, and 326 are located to the outside of the bond pads 310 through 317. That is, the driver/ESD cells 320, 322, 324, and 326 are located between the bond pads 310, 312, 314, and 316 and the die edge 360. This driver/ESD cell layout has the advantage of allowing the metal connections between the bond pads 310, 312, 314, and 316 and their associated driver/ESD cells 320, 322, 324, and 326 to be as wide as the metal connections between the bond pads 311, 323, 325, and 327 and their associated drive/ESD cells 321, 323, 325, and 327. These metal connections may have a

width of 80 microns, although other embodiments are possible with other metal connection widths. The driver/ESD layout of this example embodiment also allows the driver/ESD cells to have widths greater than those possible with prior integrated circuits.

The pre-driver/receiver cells 330 through 337 are electrically connected to the driver/ESD cells 320 through 327 by way of a series of electrically conductive paths, two of which have been labeled in figure 3 as 350 and 357. These electrically conductive paths may have a width of approximately 1 to 2 microns, although other embodiments are possible with other widths. The electrically conductive paths connecting pre-driver/receiver cells 330, 332, 334, and 336 to driver/ESD cells 320, 322, 324, and 326 may be routed between the bond pads 310 through 317 and between the driver/ESD cells 321, 323, 325, and 327. It is also possible to route these electrically conductive paths on another layer underneath the driver/ESD and bond pad structures. Because the electrically conductive paths between the pre-driver cells 330, 332, 334, and 336 and the driver/ESD cells 320, 322, 324, and 326 are relatively narrow, perhaps 1 or 2 microns in width, the electrically conductive paths may be routed underneath the bond pads without creating an additional risk of cracking inter layer dielectric material during installation of bond wires. Further, although figure 3 shows only one electrically conductive path between each pre-driver/receiver cell and its associated driver/ESD cell, other embodiments are possible with more than one electrically conductive path between each pre-driver/receiver cell and its associated driver/ESD cell.

Figure 4 is a flow diagram of an embodiment of a method for optimizing driver cell layout in a staggered bond pad integrated circuit. At step 410, a plurality of bond pads on a die are configured into an array. At step 420, a first plurality of driver cells are placed to the outside of the plurality of bond pads. That is, the first plurality of driver cells are situated between the bond pads and the nearest edge of the die. At step 430, a second plurality of driver cells are placed to the inside of the plurality of bond pads. That is, the second plurality of driver cells are situated between the bond pads and the die core.

In the foregoing specification the invention has been described with reference to specific exemplary embodiments thereof. It will, however, be evident that various modifications and changes may be made thereto without departing from the broader spirit and scope of the invention as set forth in the appended claims. The specification and drawings are, accordingly, to be regarded in an illustrative rather than in a restrictive sense.

CLAIMS

What is claimed is:

1. An apparatus, comprising:

a plurality of bond pads configured in an array;

a first plurality of driver cells located to the outside of the plurality of bond pads; and

a second plurality of driver cells located to the inside of the plurality of bond pads.

2. The apparatus of claim 1, wherein the plurality of bond pads are configured in a staggered array.

3. The apparatus of claim 2, further comprising a plurality of pre-drive cells located to the inside of the second plurality of driver cells.

4. The apparatus of claim 3, wherein the plurality of bond pads are configured in a staggered array including an inner ring and an outer ring of bond pads.

5. The apparatus of claim 4, further comprising a plurality of metal connections, each of the plurality of metal connections to couple one of the first and second pluralities of driver cells to one of the plurality of bond pads.

6. The apparatus of claim 5, further comprising a plurality of conductive interconnects, each of the plurality of pre-driver cells coupled to one of the first and second pluralities of driver cells by at least one of the plurality of conductive interconnects.

7. The apparatus of claim 6, each the plurality of conductive interconnects substantially more narrow in width than each of the plurality of metal connections.

8. The apparatus of claim 7, the first and second pluralities of driver cells each having a width of approximately 80 microns.

9. A semiconductor device, comprising:

a die including

a plurality of bond pads configured in an array;

a first plurality of driver cells located to the outside of the plurality of bond pads, and

a second plurality of driver cells located to the inside of the plurality of bond pads; and

a lead frame including a plurality of lead fingers, the plurality of lead fingers coupled the plurality of bond pads by a plurality of bond wires.

10. The semiconductor device of claim 9, wherein the plurality of bond pads are configured in a staggered array.

11. The semiconductor device of claim 10, further comprising a plurality of pre-drive cells located to the inside of the second plurality of driver cells.

12. The semiconductor device of claim 11, wherein the plurality of bond pads are configured in a staggered array including an inner ring and an outer ring of bond pads.

13. The semiconductor device of claim 12, further comprising a plurality of metal connections, each of the plurality of metal connections to couple one of the first and second pluralities of driver cells to one of the plurality of bond pads.

14. The semiconductor device of claim 13, further comprising a plurality of conductive interconnects, each of the plurality of pre-driver cells coupled to one of the first and second pluralities of driver cells by at least one of the plurality of conductive interconnects.

15. The semiconductor device of claim 14, each the plurality of conductive interconnects substantially more narrow in width than each of the plurality of metal connections.

16. The semiconductor device of claim 15, the first and second pluralities of driver cells each having a width of approximately 80 microns.

17. A method, comprising:

configuring a plurality of bond pads on a die in an array;

placing a first plurality of driver cells to the outside of the plurality bond pads; and

placing a second plurality of driver cells to the inside of the plurality of bond pads.

18. The method of claim 17, wherein configuring the plurality of bond pads in an array includes configuring the plurality of bond pads in a staggered array.

19. The method of claim 18, further comprising placing a plurality of pre-driver cells to the inside of the plurality of bond pads.

20. The method of claim 19, further comprising electrically coupling each of the plurality of pre-driver cells to one of the first and second plurality of driver cells.

21. The method of claim 20, further comprising connecting each of the plurality of bond pads to one of a plurality of lead fingers on a lead frame.

ABSTRACT OF THE DISCLOSURE

An embodiment of an integrated circuit die with staggered bond pads and optimized driver layout includes a staggered array of bond pads with an outer ring of bond pads and an inner ring of bond pads. Driver/ESD circuit cells for the outer ring of bond pads are located to the outside of the bond pads (between the outer ring of bond pads and the nearest die edge). The driver/ESD cells for the inner ring of bond pads are located to the inside of the bond pads (between the inner ring of bond pads and the die core).

100

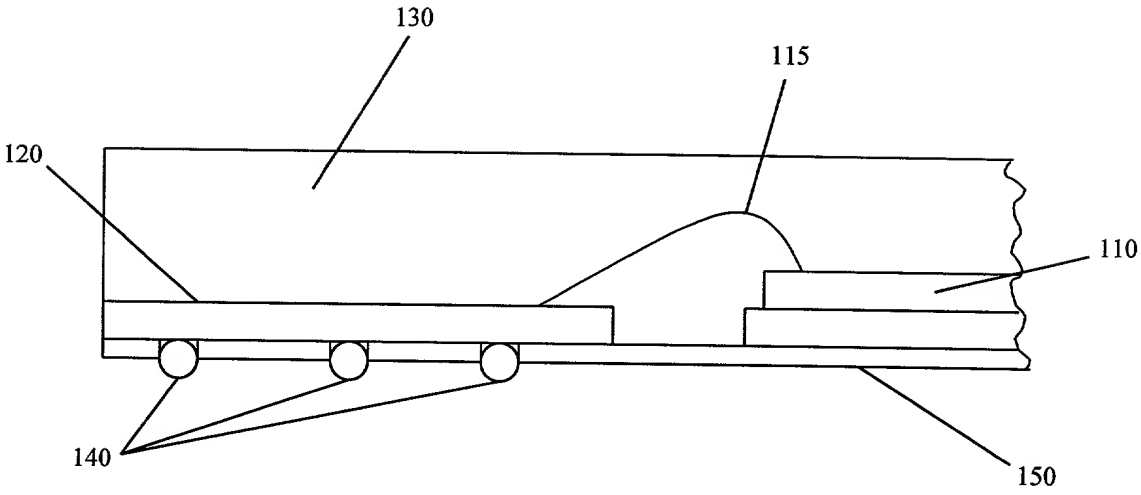

Figure 1 - Prior Art

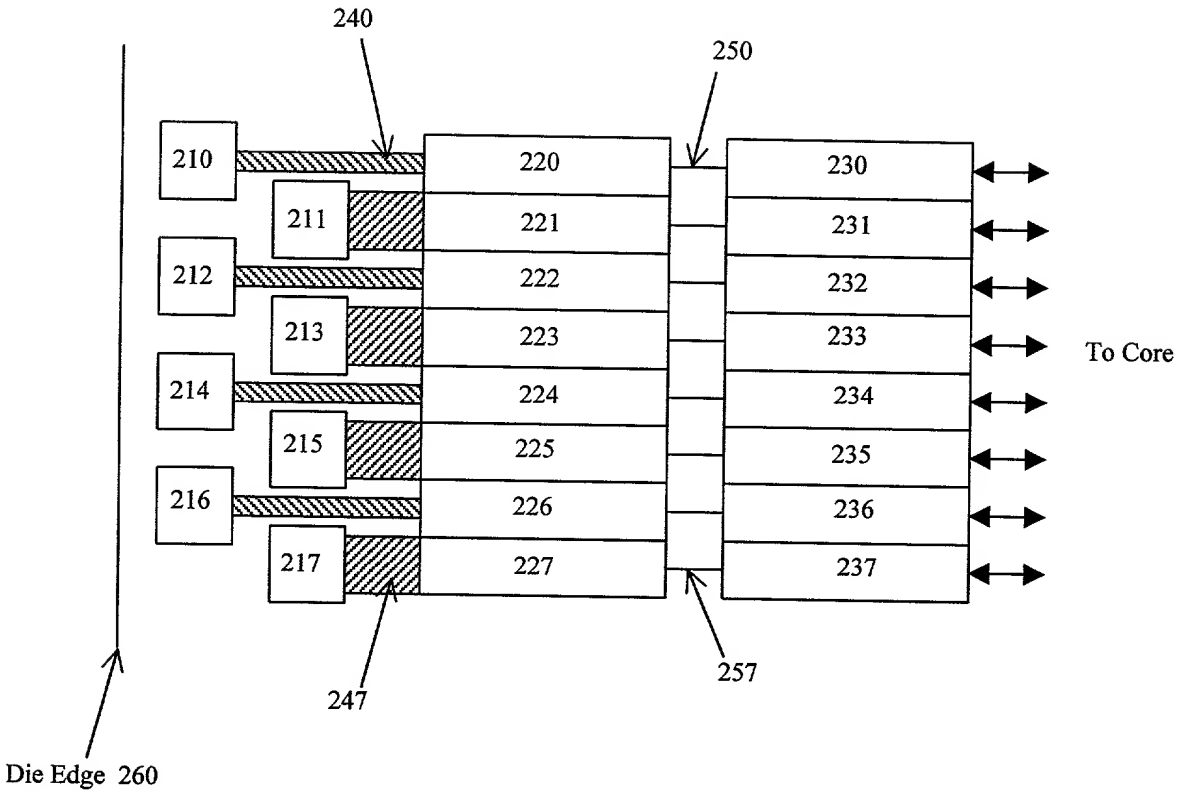

Figure 2 – Prior Art

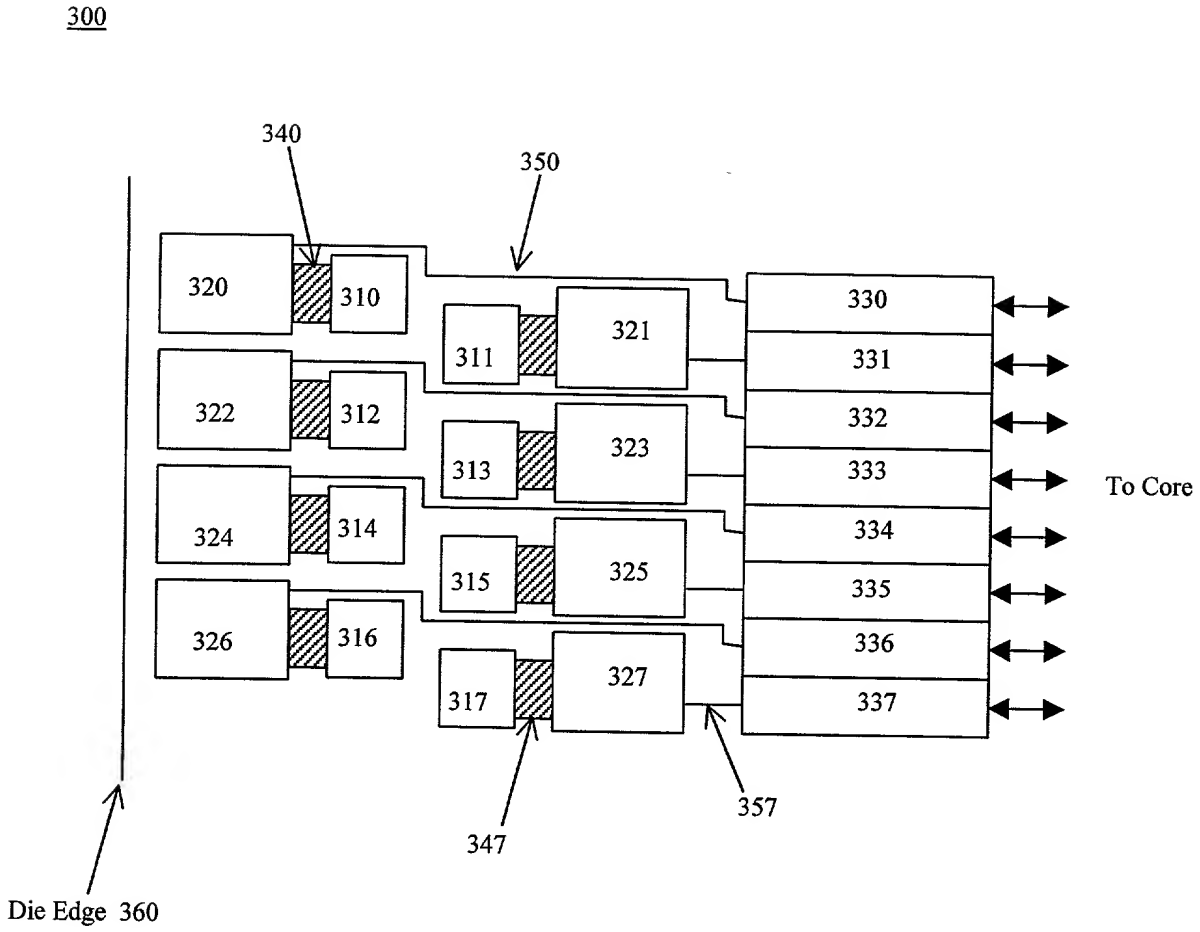
300
340
350
320
310
311
321
330
331
322
312
332
313
323
333
To Core
324
314
334
315
325
335
326
316
336
317
327
337
357
347
Die Edge 360

Figure 3

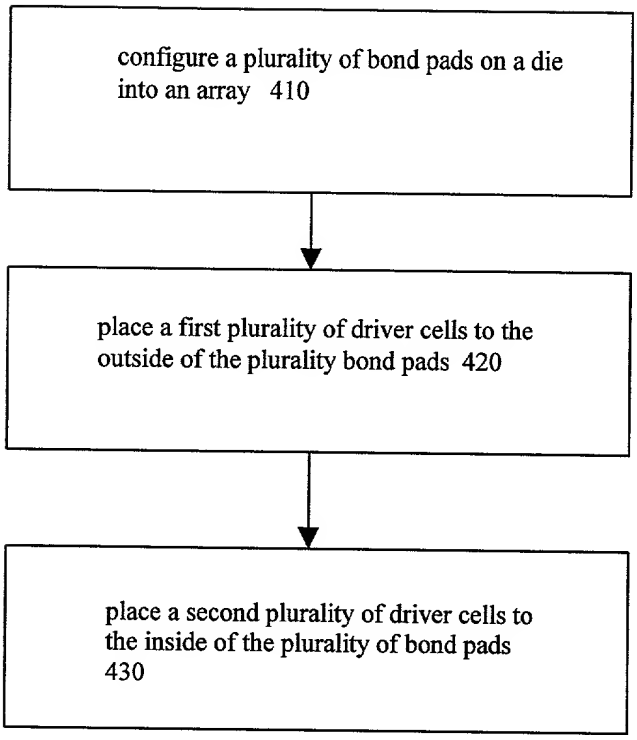
configure a plurality of bond pads on a die into an array 410
place a first plurality of driver cells to the outside of the plurality bond pads 420
place a second plurality of driver cells to the inside of the plurality of bond pads 430

Figure 4

Attorney's Docket No.: 042390.P7143 PATENT

DECLARATION AND POWER OF ATTORNEY FOR PATENT APPLICATION
(FOR **INTEL CORPORATION** PATENT APPLICATIONS)

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below, next to my name.

I believe I am the original, first, and sole inventor (if only one name is listed below) or an original, first, and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled
Optimized Driver Layout For Integrated Circuits With Staggered Bond Pads.

the specification of which

_X_ is attached hereto.
___ was filed on _____ as
United States Application Number _____
or PCT International Application Number _____
and was amended on _____.
(if applicable)

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claim(s), as amended by any amendment referred to above. I do not know and do not believe that the claimed invention was ever known or used in the United States of America before my invention thereof, or patented or described in any printed publication in any country before my invention thereof or more than one year prior to this application, that the same was not in public use or on sale in the United States of America more than one year prior to this application, and that the invention has not been patented or made the subject of an inventor's certificate issued before the date of this application in any country foreign to the United States of America on an application filed by me or my legal representatives or assigns more than twelve months (for a utility patent application) or six months (for a design patent application) prior to this application.

I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, Section 119(a)-(d), of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed:

Prior Foreign Application(s)			Priority Claimed	
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No
(Number)	(Country)	(Day/Month/Year Filed)	Yes	No

I hereby claim the benefit under Title 35, United States Code, Section 119(e) of any United States provisional application(s) listed below:

Application Number	Filing Date
Application Number	Filing Date

I hereby claim the benefit under Title 35, United States Code, Section 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, Section 112, I acknowledge the duty to disclose all information known to me to be material to patentability as defined in Title 37, Code of Federal Regulations, Section 1.56 which became available between the filing date of the prior application and the national or PCT international filing date of this application:

Application Number	Filing Date	Status -- patented, pending, abandoned
Application Number	Filing Date	Status -- patented, pending, abandoned

I hereby appoint the persons listed on Appendix A hereto (which is incorporated by reference and a part of this document) as my respective patent attorneys and patent agents, with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith.

Send correspondence to John P. Ward **(Name of Attorney or Agent)**, **BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP, 12400 Wilshire Boulevard 7th Floor, Los Angeles, California 90025 and direct telephone calls to** John P. Ward **(Name of Attorney or Agent)**, **(408) 720-8598.**

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Full Name of Sole/First Inventor Michael A. Jassowski

Inventor's Signature _____ Date _____

Residence El Dorado, California (City, State) Citizenship USA (Country)

Post Office Address 4808 East China Hill Road
El Dorado, California 95623

William E. Alford, Reg. No. 37,764; Farzad E. Amini, Reg. No. P42,261; Aloysius T. C. AuYeung, Reg. No. 35,432; William Thomas Babbitt, Reg. No. 39,591; Carol F. Barry, Reg. No. 41,600; Jordan Michael Becker, Reg. No. 39,602; Bradley J. Bereznak, Reg. No. 33,474; Michael A. Bernadicou, Reg. No. 35,934; Roger W. Blakely, Jr., Reg. No. 25,831; Gregory D. Caldwell, Reg. No. 39,926; Ronald C. Card, Reg. No. P44,587; Thomas M. Coester, Reg. No. 39,637; Stephen M. De Klerk, under 37 C.F.R. § 10.9(b); Michael Anthony DeSanctis, Reg. No. 39,957; Daniel M. De Vos, Reg. No. 37,813; Robert Andrew Diehl, Reg. No. 40,992; Matthew C. Fagan, Reg. No. 37,542; Tarek N. Fahmi, Reg. No. 41,402; James Y. Go, Reg. No. 40,621; James A. Henry, Reg. No. 41,064; Willmore F. Holbrow III, Reg. No. P41,845; Sheryl Sue Holloway, Reg. No. 37,850; George W Hoover II, Reg. No. 32,992; Eric S. Hyman, Reg. No. 30,139; Dag H. Johansen, Reg. No. 36,172; William W. Kidd, Reg. No. 31,772; Erica W. Kuo, Reg. No. 42,775; Michael J. Mallie, Reg. No. 36,591; Andre L. Marais, under 37 C.F.R. § 10.9(b); Paul A. Mendonsa, Reg. No. 42,879; Darren J. Milliken, Reg. 42,004; Lisa A. Norris, Reg. No. P44,976; Chun M. Ng, Reg. No. 36,878; Thien T. Nguyen, Reg. No. 43,835; Thinh V. Nguyen, Reg. No. 42,034; Dennis A. Nicholls, Reg. No. 42,036; Kimberley G. Nobles, Reg. No. 38,255; Daniel E. Ovanezian, Reg. No. 41,236; Babak Redjaian, Reg. No. 42,096; William F. Ryann, Reg. 44,313; James H. Salter, Reg. No. 35,668; William W. Schaal, Reg. No. 39,018; James C. Scheller, Reg. No. 31,195; Jeffrey Sam Smith, Reg. No. 39,377; Maria McCormack Sobrino, Reg. No. 31,639; Stanley W. Sokoloff, Reg. No. 25,128; Judith A. Szepesi, Reg. No. 39,393; Vincent P. Tassinari, Reg. No. 42,179; Edwin H. Taylor, Reg. No. 25,129; John F. Travis, Reg. No. 43,203; George G. C. Tseng, Reg. No. 41,355; Joseph A. Twarowski, Reg. No. 42,191; Lester J. Vincent, Reg. No. 31,460; Glenn E. Von Tersch, Reg. No. 41,364; John Patrick Ward, Reg. No. 40,216; Charles T. J. Weigell, Reg. No. 43,398; Kirk D. Williams, Reg. No. 42,229; James M. Wu, Reg. No. P45,241; Steven D. Yates, Reg. No. 42,242; Ben J. Yorks, Reg. No. 33,609; and Norman Zafman, Reg. No. 26,250; my patent attorneys, and Andrew C. Chen, Reg. No. 43,544; Justin M. Dillon, Reg. No. 42,486; Paramita Ghosh, Reg. No. 42,806; and Sang Hui Kim, Reg. No. 40,450; my patent agents, of BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP, with offices located at 12400 Wilshire Boulevard, 7th Floor, Los Angeles, California 90025, telephone (310) 207-3800, and Alan K. Aldous, Reg. No. 31,905; Robert D. Anderson, Reg. No. 33,826; Joseph R. Bond, Reg. No. 36,458; Richard C. Calderwood, Reg. No. 35,468; Jeffrey S. Draeger, Reg. No. 41,000; Cynthia Thomas Faatz, Reg No. 39,973; Sean Fitzgerald, Reg. No. 32,027; Seth Z. Kalson, Reg. No. 40,670; David J. Kaplan, Reg. No. 41,105; Charles A. Mirho, Reg. No. 41,199; Leo V. Novakoski, Reg. No. 37,198; Naomi Obinata, Reg. No. 39,320; Thomas C. Reynolds, Reg. No. 32,488; Kenneth M. Seddon, Reg. No. 43,105; Mark Seeley, Reg. No. 32,299; Steven P. Skabrat, Reg. No. 36,279; Howard A. Skaist, Reg. No. 36,008; Steven C. Stewart, Reg. No. 33,555; Raymond J. Werner, Reg. No. 34,752; Robert G. Winkle, Reg. No. 37,474; and Charles K. Young, Reg. No. 39,435; my patent attorneys, and Thomas Raleigh Lane, Reg. No. 42,781; Calvin E. Wells; Reg. No. P43,256, Peter Lam, Reg. No. P44,855; and Gene I. Su, Reg. No. 45,140; my patent agents, of INTEL CORPORATION; and James R. Thein, Reg. No. 31,710, my patent attorney; with full power of substitution and revocation, to prosecute this application and to transact all business in the Patent and Trademark Office connected herewith.

APPENDIX B

Title 37, Code of Federal Regulations, Section 1.56
Duty to Disclose Information Material to Patentability

(a) A patent by its very nature is affected with a public interest. The public interest is best served, and the most effective patent examination occurs when, at the time an application is being examined, the Office is aware of and evaluates the teachings of all information material to patentability. Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability as defined in this section. The duty to disclosure information exists with respect to each pending claim until the claim is cancelled or withdrawn from consideration, or the application becomes abandoned. Information material to the patentability of a claim that is cancelled or withdrawn from consideration need not be submitted if the information is not material to the patentability of any claim remaining under consideration in the application. There is no duty to submit information which is not material to the patentability of any existing claim. The duty to disclosure all information known to be material to patentability is deemed to be satisfied if all information known to be material to patentability of any claim issued in a patent was cited by the Office or submitted to the Office in the manner prescribed by §§1.97(b)-(d) and 1.98. However, no patent will be granted on an application in connection with which fraud on the Office was practiced or attempted or the duty of disclosure was violated through bad faith or intentional misconduct. The Office encourages applicants to carefully examine:

(1) Prior art cited in search reports of a foreign patent office in a counterpart application, and

(2) The closest information over which individuals associated with the filing or prosecution of a patent application believe any pending claim patentably defines, to make sure that any material information contained therein is disclosed to the Office.

(b) Under this section, information is material to patentability when it is not cumulative to information already of record or being made or record in the application, and

(1) It establishes, by itself or in combination with other information, a prima facie case of unpatentability of a claim; or

(2) It refutes, or is inconsistent with, a position the applicant takes in:

(i) Opposing an argument of unpatentability relied on by the Office, or

(ii) Asserting an argument of patentability.

A prima facie case of unpatentability is established when the information compels a conclusion that a claim is unpatentable under the preponderance of evidence, burden-of-proof standard, giving each term in the claim its broadest reasonable construction consistent with the specification, and before any consideration is given to evidence which may be submitted in an attempt to establish a contrary conclusion of patentability.

(c) Individuals associated with the filing or prosecution of a patent application within the meaning of this section are:

(1) Each inventor named in the application;

(2) Each attorney or agent who prepares or prosecutes the application; and

(3) Every other person who is substantively involved in the preparation or prosecution of the application and who is associated with the inventor, with the assignee or with anyone to whom there is an obligation to assign the application.

(d) Individuals other than the attorney, agent or inventor may comply with this section by disclosing information to the attorney, agent, or inventor.